NanoSpice CCK

PRIMARIUS

Advanced CCK Analysis Tool

Introduction

NanoSpice CCK is an advanced circuit check tool that provides comprehensive transistor-level ERC and SOA circuit check. It is suitable for both pre-layout and post-layout simulation, and can quickly generate accurate test results, making it convenient for designers to detect potential design issues, such as leakage and high resistance, in a timely manner.

NanoSpice CCK supports static circuit checks and dynamic circuit checks based on transient simulation. The static circuit check includes a rich set of functions such as power domain check, etc. Empowered by the innovative static voltage propagation algorithm, NanoSpice CCK can flexibly and accurately handle voltage propagation problems at complex power domain boundaries, such as high voltage and negative voltage, providing customers with accurate and reliable detection results. Dedicated to avoiding common defects caused by improper design practices, NanoSpice CCK provides comprehensive verification of circuit reliability during the circuit design phase. The dynamic circuit check function, based on transient simulation, includes commonly used circuit checks such as device current check, which can be used in analog and digital cosim simulations. Leveraging the efficient parallel NanoSpice simulator for transient simulation, NanoSpice CCK can efficiently and accurately detect abnormal circuit operation under different stimuli, and provide a convenient waveform comparison function, facilitating users in quickly locating and resolving problems.

Specifications

Static circuit check	Dynamic circuit check	Supported	
Static voltage	High impedance state node	\otimes	
Static HiZ node	DC path	\otimes	
Static DC path	Leakage current path by HiZ nodes	\otimes	
Static MOS voltage	Block power	\otimes	
Static device operating	Device current	\otimes	
Static ERC	Active/inactive nodes	\otimes	
Power gating	Device operation points	\otimes	
Forward bias	Rise/fall transition time	\otimes	
Dangling node	Timing setup/hold/delay/width	\otimes	
Transmission gate	Expression	\otimes	
Fan-out	Dynamic glitch	\otimes	
Beta ratio		\otimes	

NanoSpice CCK

Comprehensive

- Static & dynamic check
- Compatible with third-party tools

Accurate

- Voltage propagation algorithm
- Multiple circuit check rules

Efficient

- Advanced infra-structure
- Multi-core parallel technology

User-friendly

- Classification & redundant removal
- · Waveform & CCK report mutual check

Key Advantages

High-performance

Innovative algorithms for static voltage propagation, high resistance state detection, and leakage path search

Multiple methods for classification and redundancy removal of simulation results

Parallel simulation

Both static and dynamic checks support multiple parallel checks to reduce run time

Large capacity

Leading technology minimizes performance and memory consumption overhead of dynamic checks

Compatibility

Rich and complete features that can be quickly migrated from existing tools

User-friendly

Easy to use

Applications

- Block level analog to full chip SoC circuit check
- Full chip memory (SRAM, DRAM, Flash) circuit check
- · Full custom digital circuit check

Application Examples

Faster speed with more accurate report and less missing/false violations

Circuit Types Test Cases	Circuit Check Types	Reference	NanoSpice CCK	Speedup	
	Test Cases	Circuit Check Types	Run Time (hours)		
Dynamic circuit check 16Mb NOR Flash	Dynamic DC path	27.1	4.2	6.5X	
	Dynamic expression	15.8	6.1	2.6X	
	Dynamic device opration points	16.2	6.1	2.6X	
Static circuit check	100 pre-layout cases with up to 70 million MOSFETs	DC path, HiZ node, devop, forward bias, fan-out, beta ratio, dangling node & power gating static CCK types	58	30	1.9X